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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,603	04/14/2005	Paulus Petrus Franciscus Maria Bruin	NL 021020	8229

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/531,603	BRUIN ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/27/2006; 4/14/05.*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 4 rejected under 35 U.S.C. 102(b) as being anticipated by Bucksch (US 5600176).

3. With respect to claim 1, figures 1 and 2 of Bucksch disclose a voltage divider arrangement comprising a reference terminal (2), an input terminal (1) for receiving an input signal with respect to said reference terminal (2), an output terminal (3) for supplying an output signal with respect to said reference terminal (2), and a resistor arrangement (R1.1-R1.6 and R2.1-R2.6) arranged on a substrate (5) and coupled between said input terminal (1) and said reference terminal (1), wherein a distributed compensation capacitance structure (4) for compensating the influence of a distributed parasitic capacitance is arranged between said resistor arrangement (R1.1-R1.6 and R2.1-R2.6) and said substrate (5).

With respect to claim 2, figures 1 and 2 of Bucksch disclose a voltage divider arrangement according to claim 1, wherein said resistor arrangement has a meandering shape.

With respect to claim 4, figures 2 and 3 disclose a voltage divider arrangement according to claim 1, wherein said distributed compensation capacitance structure (4)

comprises a conductor layer of a predetermined shape.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Der Zee in view of Bucksch.

With respect to claim 1, figures 2, 5, 6 and 7 of Van Der Zee disclose a voltage divider arrangement comprising a reference terminal (going into 1), an input terminal (going into 2) for receiving an input signal with respect to said reference terminal (going into 1), an output terminal (3) for supplying an output signal with respect to said reference terminal (going into 1), and a resistor arrangement (R1-RM+1) arranged on a substrate (SBSTR) and coupled between said input terminal (going into 2) and said reference terminal (going into 1), but fails to disclose wherein a distributed compensation capacitance structure for compensating the influence of a distributed parasitic capacitance is arranged between said resistor arrangement (R1-RM+1) and said substrate (SBSTR). Figures 2 and 3 of Bucksch teaches the use of a layer compensation capacitance structure (4) for compensating the influence of a distributed parasitic capacitance is arranged between a resistor arrangement and a substrate. It

would have been obvious to one skilled at the time the invention was made to a person having ordinary skill in the art to use the teaching of Bucksch in the structure of Van Der Zee for the purpose of frequency compensation.

With respect to claim 2, the above combination discloses a voltage divider arrangement according to claim 1, wherein said resistor arrangement has a meandering shape.

With respect to claim 3, the above combination discloses a voltage divider arrangement according to claim 2, wherein said resistor arrangement is made of poly-silicon (see column 4 lines 5-10 of Van Der Zee).

With respect to claim 4, the above combination discloses a voltage divider arrangement according to claim 1, wherein said distributed compensation capacitance structure (4) comprises a conductor layer of a predetermined shape.

With respect to claim 5, the above combination (in figures 6 and 7 of Van Der Zee) disclose a voltage divider arrangement according to claim 4, wherein said predetermined shape is a triangular shape.

With respect to claim 7, the above combination discloses a voltage divider arrangement according to claim 1, wherein said distributed compensation capacitance structure (4) is separated from said resistor arrangement and said substrate (SBSTR) by respective insulation layers.

Allowable Subject Matter

1. Claim 6 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 6, the prior art of record fails to suggest or disclose the voltage divider arrangement wherein the width of said conductor layer in the horizontal direction is selected according to the equation D k = DR 1 + k M + 1 - k CCMP sq CP sq ,wherein CP.sub.sq denotes the parasitic capacitance per unit area of resistor, DR denotes the length of said resistor arrangement (20), k denotes an index of a segment of said transistor arrangement (20); M denotes the total number of segments of said transistor arrangement (20), CCMP.sub.sq denotes the distributed compensation capacitance per unit area of resistor and D.sub.k denotes said width of said conductor layer.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
8/4/2006

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QUAN TRA
PRIMARY EXAMINER